## REMARKS

This is in response to the Office Action dated April 8, 2008. Claims 1-3, 5-23 and 25 are pending. Claims 1, 6 and 8 stand rejected in the outstanding Office Action. Claims 2-3, 5, 7, 9-23 have been withdrawn. Claim 1 has been amended. New claim 25 has been added.

The objection of claims 1, 6 and 8 for informalities is respectfully traversed. The language of claim 1 has been amended appropriately to make it clear that the second cell drives both the logic operation circuit and the data retaining circuit (a situation identified as "meaning B" by the Examiner), see for example Fig. 4.

The rejection of independent claim 1 as allegedly being anticipated under 35 U.S.C. § 102(b) by Kajigaya et al. (US 5,151,881) is respectfully traversed. Kajigaya fails to disclose or even remotely suggest each and every limitation set forth in the claims. Anticipation requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference", *Verdegaal Bro. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987) (MPEP § 2131).

Kajigaya generally discloses a memory array M-ARY used in a semiconductor memory (Fig. 1). The memory array is connected to peripheral circuits, including a column address buffer CADB, a column address decoder CDCR, and a column switch CSW (col. 4, lines 27-66). The column address buffer CADB incorporates and holds Y-address signals supplied through external terminals A0 to Ai, forms complementary internal address signals ay0 to ayi on the basis of the Y-address signals and supplies said signals ay0 to ayi to the column address decoder CDCR. The column address decoder CDCR decodes the received signals ay0 to ayi and forms data line select signals Y0 to Yn in synchronism with a timing signal φy, and supplies them to corresponding switching MOSFETs in the column switch CSW. The column switch CSW

consists of n+1 pairs of switching MOSFETs in correspondence with the pairs of the complementary data lines. CSW selectively connects a pair of complementary data lines designated by column address signals Y0 to Yn to the common complementary data lines CD and CD inverse.

The column address buffer CADB is shown in Fig. 2 (col. 8, lines 44-62). It comprises multiple units IC0 to ICi, each of said units comprising a pair of PMOS transistors Q1 and Q2 connected in series and connected to a pair of NMOS transistors Q11 and Q12 also connected in series. The source of Q1 is connected to voltage Vcc, and the source of Q12 is grounded. Moreover, the gates of Q1 and Q12 are connected to input A0, whereas the gate of Q2 is connected to a first control signal (from N2), and the gate of Q11 is connected to a second control signal (from N1), which is inverse of the first control signal.

The Examiner identified the column address decoder CDCR as the first cell, and the column address buffer CADB as the second cell. According to the Examiner "the second cell CADB functions as a driver circuit…for driving a circuit comprising the logic operation circuit CDCR and a data retaining circuit CSW for retaining data output by the logic operation circuit CDCR".

First, the column switch element CSW, identified by the Examiner as a "data retaining circuit" is not a data retaining circuit. CSW is simply a switch that selectively connects the inputs Y0 to Yn to the two common complementary data lines CD and inverse of CD (lines 42-46, col. 4). In contrast, in an example embodiment disclosed in the present application, the data retaining circuit is a data flip-flop which is a primitive memory cell, retaining input data for a period of time before it outputs it.

Second, the column address decoder CDCR, has been identified by the Examiner as a "logic operation circuit". It does not appear from the description given in Kajigaya that said element CDCR performs any logic operation. According to Kajigaya, the CDCR decodes received signals ay0 to ayi supplied from the column address buffer CADB and forms signals Y0 to Yn for sending to the column switch element CSW. In contrast, in an example embodiment, the logic operation circuit 2, comprising the first cell S1 (see Fig. 4 in the specification), performs a logic operation on the input signals (line 22, p. 45 to line 1, p. 46 in the specification).

For the above reasons, independent claim 1 is allowable.

Regarding claim 8, the source of the first NMOS transistor Q12 in Kajigaya's device is grounded (col. 8, lines 44-49) and not connected to a second source voltage, as required by claim 8.

New claim 25 recites the limitation that "the data retaining circuit comprises a data flip-flop circuit". Support can be found in page 48, lines 21-23 of the specification. Kajigaya fails to teach this feature.

It is respectfully requested that the rejection of claims 6, 8 and 24, each being dependent from claim 1, also be withdrawn.

In view of the foregoing and other considerations, all claims are deemed in condition for allowance. A formal indication of allowability is earnestly solicited.

The Commissioner is authorized to charge the undersigned's deposit account #14-1140 in whatever amount is necessary for entry of these papers and the continued pendency of the captioned application.

Should the Examiner feel that an interview with the undersigned would facilitate allowance of this application, the Examiner is encouraged to contact the undersigned.

Respectfully submitted,

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